REMARKS

Claims 1-31 are pending in this application. Applicants thank the Examiner for the indication that claims 4, 11, and 20 would be allowable if rewritten in independent form. By this response, claims 15-17 and 19 are canceled without prejudice or disclaimer. Claim 20 is amended by rewriting the claim into independent form. Claims 18, 21, and 22 are amended to show a change in dependencies as brought about by rewriting claim 20 in independent form. Applicant respectfully requests that the above-identified application be reconsidered in view of the following remarks.

Drawing Objections

The Office Action objected to the drawings because a descriptive label does not identify all elements illustrated in the figures. The Office specifically identified that element 420 is not identified as "dispatcher." Applicants assert that the drawings are understandable as they stand and descriptive labels are not required, however, in accordance with the requirement of the Office, elements 410 and 420 have been modified to include descriptive labels of "allocator" and "dispatcher," respectively.

The 35 U.S.C. § 103 Rejection

Claims 1 and 28:

Claims 1 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,449,701 to Cho ("Cho") in view of U.S. Patent No. 6,272,600 to Talbot et al. ("Talbot").

Cho relates to a memory controller that includes a request queue for receiving transaction information and a channel control circuit. A control circuit for the request queue may issue addresses from the request queue to the channel control circuit out of order, and thus the memory operations may be completed out of order. Cho, however, fails to teach at least "simultaneously monitor[ing] a status of said plurality of data requests," as recited in claim 1, or "simultaneously monitoring a status of each of said data requests to a plurality of memory locations," as similarly recited in claim 28. The Office Action asserts that Cho teaches these features in columns 4-10, and figure 2. The

Office Action states "[c]ompare circuitry in request queue 40 sets an issued indication (Iss) to a state indicating that the transaction has been issued" and asserts that this is a teaching of "simultaneously monitoring a status of said plurality of data requests" as recited in claim 1 and similarly recited in claim 28. However, Cho actually discloses that "Compare circuitry in request queue 40 may compare the data buffer pointers (Ptr) returned by channel control circuit 42A to the data buffer pointers in each queue entry to identify which transaction is being acknowledged, and an issued notification ... may be set to a state indicating that the transaction has been issued." Col. 8, lines 4-10. Thus, the portion of Cho relied on by the Office discloses monitoring of the data buffer pointers (Ptr) returned by channel control circuit 42A and fails to disclose simultaneous monitoring of a status of a plurality of data requests. Moreover, control circuit 50 issues transactions to the control circuit 42A for access to memory 26. Col. 7, lines 39-41. By identifying which transaction is being acknowledged, the compare circuitry is not monitoring the status of a data request in the buffer, rather, it is monitoring activities occurring outside of the buffer, namely in the memory. Accordingly, Cho fails to teach or suggest "simultaneously monitor[ing] a status of said plurality of data requests," as recited in claim 1, or "simultaneously monitoring a status of each of said data requests to a plurality of memory locations," as similarly recited in claim 28.

Talbot does not cure the deficiencies of Cho. Talbot relates to a system that carries out memory transactions in an order that maximizes concurrency in a memory system such as a multi-bank interleaved memory system. Read data is collected in a buffer memory to be presented back to the bus in the same order as read transactions were requested, even though requests had been presented to the memory system in a different order. Talbot is devoid of any teaching or suggestion of "simultaneously monitor[ing] a status of said plurality of data requests," as recited in claim 1, or "simultaneously monitoring a status of each of said data requests to a plurality of memory locations," as similarly recited in claim 28.

For at least the above reasons, claims 1 and 28, and all claims dependent thereon, are allowable.

Claims 8-14:

In the Office Action dated May 5, 2004, all rejections based on Kazachinsky were withdrawn based on the Applicant's arguments of February 2, 2004. Office Action at para. 17). As this was the sole ground for the rejection in the previous office action and no new grounds were raised in the most recent office action, these claims are allowable.

Claims 18 and 20-23:

Claim 20 has been amended to include its independent and intervening bases. The Office Action states that in this form, claim 20 is allowable. Accordingly, claims 18 and 21-23 are allowable as dependent upon claim 20.

Claim 24:

Talbot does not disclose or suggest "obtaining data regarding said plurality of data requests from a plurality of memory devices." The Office Action states that Talbot renders claim 24 unpatentable under 35 U.S.C. § 103(a), however the Office Action does not cite to any portion of Talbot that teaches a "plurality of memory devices." Even more telling is that Talbot consistently refers to the memory subsystem as a single "black-box" entity. Figures 2A, 2B, 3A, 3B, and 4, as well as numerous portions of the description of Talbot, all indicate that the memory requests go, without exception, to the "memory subsystem 216." For example, Talbot reads: "The processors ... generate requests for the memory subsystem 216..." (Talbot, col. 3, ll. 60-61), "[t]he memory subsystem 216 begins executing *each* requested operation..." (Talbot, col. 4, ll. 40-41)(emphasis added), and "requests are submitted to the memory subsystem 216 as soon as they are scheduled" (Talbot, col. 7, ll. 26-27). Though Talbot's reordering involves rearranging requests based on memory locations, this does not teach a plurality of memory devices. A memory location is merely an addressable portion of memory, or "target memory address" in Talbot. For at least this reason, claim 24 and all claims dependent on claim 24 are allowable.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is now in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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